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REMARKS

Claims 1-20 are pending. Claims 21 and 22 are being added. No new matter is being added.

Claim 15 stands objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Appreciation is expressed for the indication of allowability of independent claim 15.

Claims 1-4, 6-10, 13, and 16-17 stand rejected under 35 U.S.C. 102(b) as being anticipated by Young et al., U.S. Patent No. 5,285,421 (Young). Claims 5, 11-12, and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Young, and further in view of Lee et al., U.S. Patent No. 5,920,504 (Lee).

In contrast to the present invention, Young does not disclose or suggest "decoding circuitry, responsive to decoding a first address, to access a first storage element of a first row of the plurality of rows, and ... responsive to decoding a second address consecutive to the first address, to access a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows," all as recited in independent claim 1.

Section 4 of the Office Action identifies the X-decoder of Figure 6 as the decoding circuitry of claims 1 and 16. Specifically, the Office Action states that "the memory has been divided into two blocks or halves independent of each other, so both blocks are accessed simultaneously but two different rows of memory ... col. 4, lines 52-68 [of Young]."

However, the X-decoder of Figure 6 is not "responsive to decoding a first address, to access a first storage element of a first row of the plurality of rows, and ..., responsive to decoding a second address consecutive to the first address, to access a second storage element of a second row of the plurality of rows." With the X-decoder of Figure 6, register banks A and B may be loaded simultaneously *upon initial access* with data from two different rows of memory cells, corresponding to two different word lines. Young Col. 4, lines 63-69. Accordingly, with the X-decoder of Figure 6, the data from the different rows of memory array 503 are accessed in

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response to an initial address and not in response to two consecutive addresses. See also Column 5 of lines 1-25 of Young where it describes how the four bytes of data from the wordline specified in the initial access are gated to register bank A, and the four bytes of data from the memory cell of the next higher word line are gated to register bank B such that the data in bank B is made available at the same time as the data in bank A. Under this mode of operation, the data in the next wordline is not accessed from memory array 503 responsive to decoding a second consecutive address. Accordingly, claim 1 is allowable over Young.

In contrast to the present invention, Young does not teach a column decoder "operable responsive to at least one of the more significant bits," all as recited by claim 6.

Page 4 of the Office Action states that Figure 6 of Young does not show a column decoder, but that Young inherently teaches a column decoder that is operable responsive to the least one of the more significant bits. Page 4 of the Office Action states that bits A0-A2 represent the most significant bits.

Applicants respectfully submit that page 4 of the Office Action is incorrect when it states that bits A0-A2 of Young represents the most significant bits. Young explicitly states that address bits A0-A2 specify *the least significant bits.* Young, Col. 4, lines 40-43. Thus, the Office Action is incorrect when it states that Young includes a column decoder that is operable responsive to at least one of the more significant bits.

If the rejection of claim 6 is to be maintained, Applicants respectfully request that the Examiner "make clear" where a column decoder operable responsive to at least one of the more significant bits is necessarily present in Young. Applicants respectfully request that the Examiner, "provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." See MPEP Section 2112, subsection entitled "Examiner Must Provide Rationale Or Evidence Tending to Show Inherency. Accordingly, claim 6 is allowable over Young.

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For reasons similar to those stated above with respect to independent claim 1, Young does not disclose or suggest "decoding circuitry, responsive to the address signal having a first address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second address consecutive to the first address, accessing a second page of a second row of the plurality of rows," all as recited in Independent claim 15.

For reasons similar to those stated for above with respect to independent claim 1, Young does not disclose or suggest "accessing, responsive to the first address, a first storage element of a first row of the plurality of rows, ... the second address consecutive to the first address," and "accessing, responsive to the second address, a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows," all as recited by independent claim 16. Accordingly, claim 16 is allowable over Young.

Each dependent claim in this application depends from an independent claim and is therefore allowable for at least this reason.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.

Respectfully submitted,

By: _____

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Claim version with marked-up changes.

21. (New) The memory system of claim 6 wherein:

the numeric address comprises a group of bits;

the row decoder is operable responsive to a first portion of the group of bits;

the column decoder is operable responsive to a second portion of the group of bits,

wherein each bit of the second portion is more significant than a least significant bit of the first portion.

22. (New) The embedded control system of claim 14 wherein:

the address signal comprises a group of bits;

the row decoder is operable responsive to a first portion of the group of bits;

the column decoder is operable responsive to a second portion of the group of bits,

wherein each bit of the second portion is more significant than a least significant bit of the first portion.

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